UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/540,952	03/31/2000	Carl A. Waldspurger	9772-291-999	1926

24341   7590   11/19/2003

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EXAMINER
KENDALL, CHUCK O

ART UNIT	PAPER NUMBER
2122	9

DATE MAILED: 11/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	09/540,952	WALDSPURGER ET AL.
	Examiner	Art Unit	
	Chuck O Kendall	2122	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 August 2003*.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-17,19-30 and 32-39* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4, 6-17,19-30, and 32-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

    a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .

4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: .

DETAILED ACTION

REMARKS

1. This Office Action is the response to the communication received on August 12, 2003. Reconsideration of the instant application is requested by Applicant. All such supporting documentation has been placed of record in the file. Claims 5,18 and 31 are cancelled and claims 1-4, 6-17,19-30, and 32-39 are pending.

    a. Previously claims 1-39, were rejected under 35 U.S.C. § 102(e) and 35 U.S.C. § 103 (a) using Levine et al. USPN 6,134,710 and Krishnaswamy 6,308,318.

    b. In this action claims 1-4,6-17,19-30, and 32-39 still remains rejected under the same grounds as stated above and in previous office action.

    c. Applicant has amended claims 1,14, & 27, and argues as stated in page 12 of 14, 1st paragraph of response dated 08/12/03, that Levine doesn't disclose teaching a **being able to <u>determine the latency of a particular instruction.</u>**

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C.

102 that form the basis for the rejections under this section made in this Office

action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. Claims 1-4, 6-10,14-17,19-23,27-30, 32-36,38 and 39 are rejected

under 35 U.S.C. 102(e) as being anticipated by Levine et al. USPN 6,134,710.

Regarding claim 1, Levine anticipates a method (Col. 14 lines 40 to Col.

17 line 15), system (Col.17, lines 20 to Col. 20, lines 3) and product (Col. 20 lines

5 - 30) of monitoring the performance of a program being executed on a

computer system, comprising:

executing the program on a computer system, the program having object

code instructions (Levine,2:30-35);

at intervals interrupting execution of the program, including delivering a

first interrupt; and (3:55-60);

in response to at least a subset of the first interrupts, determining a

latency of a particular object code instruction, storing the latency in a first

database, the particular object code instruction being executed by the computer

such that the program remains unmodified (8:4-17, for latency see stalls and

durations, also see Col. 8: 34-36, Fig. 9 and Col. 12: 53 – 57, for storing

monitored information).

Regarding claim 2 the method of claim 1 wherein said determining the latency includes:

determining an initial value of a cycle counter(8:39-44, for initial value);

performing the particular object code instruction(Levine,2:30-35);

determining a final value of the cycle counter(8:39-44, for threshold value); and

determining the latency based on the initial value and the final value (8:35-40, see time of event based transition also refer back to stalls and duration events, also see Col. 12: 53 – 57 for determining processor cycles per instruction).

Regarding claim 3 the method of claim 2 further comprising:

executing at least one instruction selected from the set consisting of (A) an instruction for ensuring that the particular object code instruction is performed after the initial value of the cycle counter is determined, and (B) an instruction for ensuring that the particular object code instruction is performed before the final value of the cycle counter is determined (8:39-44, for initial value, see figure 6, for object code).

Regarding claim 4 the method of claim 2 further comprising:

applying an adjustment to the final value (8:58-60 for adjustment, see resetting threshold value).

Regarding claim 5 see reasoning in claim 2.

Regarding claim 6 the method of claim 1 wherein the particular object code instruction has a variable execution time (7:15-25).

Regarding claim 7 the method of claim 1 wherein the particular object code instruction is a memory access instruction (8:7-9).

Regarding claim 8 the method of claim 1 wherein the computer system includes a plurality of memory units, each memory unit of the plurality of memory units having a different
range of access times, and further comprising:

associating the particular object code instruction with a memory unit in

accordance with the latency and the range of access times for the memory unit
(8:5-35).

Regarding claim 9 the method of claim 1 wherein said determining the
latency includes:

determining an initial value of a cycle counter (8:39-44, for initial value);

executing a first dependent instruction to provide a predetermined
execution order (4:25-30);

performing the particular object code instruction(Levine,2:30-35);

executing a second dependent instruction to provide the predetermined
execution order (4:25-30 and see preload order);

determining a final value of the cycle counter(8:39-44, for threshold value);
and

determining the latency based on the initial value and the final value (8:35-
40, see time of event based transition also refer back to stalls and duration
events also see Col. 12: 53 – 57 for determining processor cycles per
instruction).

Regarding claim 10 the method of claim 9 wherein the first and second
dependent -instructions are memory barrier instructions (8:27-37, see registers).

Regarding claim 14, Examiner is applying the same rationale to claim,
which is the product version of the method claim as discussed in claim 1 above.

Regarding claim 15, Examiner is applying the same rationale to claim,
which is the product version of the method claim as discussed in claim 2 above.

Regarding claim 16, Examiner is applying the same rationale to claim,
which is the product version of the method claim as discussed in claim 3 above.

Regarding claim 17, Examiner is applying the same rationale to claim,
which is the product version of the method claim as discussed in claim 4 above.

Regarding claim 18, Examiner is applying the same rationale to claim,
which is the product version of the method claim as discussed in claim 5 above.

Regarding claim 19, Examiner is applying the same rationale to claim,
which is the product version of the method claim as discussed in claim 6 above.

Regarding claim 20, Examiner is applying the same rationale to claim, which is the product version of the method claim as discussed in claim 7 above.

Regarding claim 21, Examiner is applying the same rationale to claim, which is the product version of the method claim as discussed in claim 8 above.

Regarding claim 22, Examiner is applying the same rationale to claim, which is the product version of the method claim as discussed in claim 9 above.

Regarding claim 23, Examiner is applying the same rationale to claim, which is the product version of the method claim as discussed in claim 10 above.

Regarding claim 27, Examiner is applying the same rationale to claim, which is the system version of the method claim as discussed in claim 1 above.

Regarding claim 28, Examiner is applying the same rationale to claim, which is the system version of the method claim as discussed in claim 2 above.

Regarding claim 29, Examiner is applying the same rationale to claim, which is the system version of the method claim as discussed in claim 3 above.

Regarding claim 30, Examiner is applying the same rationale to claim, which is the system version of the method claim as discussed in claim 4 above.

Regarding claim 31, Examiner is applying the same rationale to claim, which is the system version of the method claim as discussed in claim 5 above.

Regarding claim 32, Examiner is applying the same rationale to claim, which is the system version of the method claim as discussed in claim 6 above.

Regarding claim 33, Examiner is applying the same rationale to claim, which is the system version of the method claim as discussed in claim 7 above.

Regarding claim 34, Examiner is applying the same rationale to claim, which is the system version of the method claim as discussed in claim 8 above.

Regarding claim 35, Examiner is applying the same rationale to claim, which is the system version of the method claim as discussed in claim 9 above.

Regarding claim 36, Examiner is applying the same rationale to claim, which is the system version of the method claim as discussed in claim 10 above.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis

for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 11-13,24-26, & 37-39 are rejected under 35 U.S.C. 103(a) as

being unpatentable over Levine et al. USPN 6,134,710 in view of Krishnaswamy

USPN 6,308,318.

Regarding claim 11 Levine discloses all the claimed limitations as applied

in claim 1. Levine doesn't explicitly disclose interpreting the instructions of the at

least one issue block and wherein said particular object code instruction is in the

issue block. However, Krishnaswamy does disclose this feature (5:45-55).

Therefore it would have been obvious to one of ordinary skill in the art at the time

the invention was made to modify Levine with Krishnaswamy, because it

transparently migrates old software into a new platform that can be executed on

a new machine, (Krishnaswamy, 1:15-20).

Regarding claim 12 the method of claim 11 wherein said interpreting

emulates a machine language instruction set of the computer system

(Krishnaswamy, 4:1-5 for emulating machine language instructions se executes).

Regarding claim 13 the method of claim 11 wherein said interpreting

updates a state of the interrupted program as though each interpreted instruction

had been directly executed by the computer system (Krishnaswamy, 4:1-5).

Regarding claim 24, Examiner is applying the same rationale to claim,

which is the product version of the method claim as discussed in claim 11 above.

Regarding claim 25, Examiner is applying the same rationale to claim,

which is the product version of the method claim as discussed in claim 12 above.

Regarding claim 26, Examiner is applying the same rationale to claim,

which is the product version of the method claim as discussed in claim 13 above.

Regarding claim 37, Examiner is applying the same rationale to claim,

which is the system version of the method claim as discussed in claim 11 above.

Regarding claim 38, Examiner is applying the same rationale to claim,

which is the system version of the method claim as discussed in claim 12 above.

Regarding claim 39, Examiner is applying the same rationale to claim,

which is the system version of the method claim as discussed in claim 13 above.

Response to Arguments

6. Applicant's arguments filed 08/12/03 have been fully considered but

they are not persuasive to over come the previous rejection.

(1) In claims 1, 14, and 27, Applicant argues that prior art doesn't teach or

disclose *determining the latency of a particular instruction*.

Response (1): Examiner believes prior art does show this functionality. As set

forth above in claim 1, Levine teaches in column 8, line 7, *monitoring* "

...execution **unit stalls and duration** (Emphasis added), execution unit idle

time...", and also in Col. 8 lines 34-36 " The state of the **execution unit is also**

saved on interrupt" (Emphasis added) and in Fig, 9 and Col. 12: 53 – 57,

Levines discloses "By using the number of processor cycles that is equivalent to

the threshold value, and by using the **average number of processor cycles**

per instruction ("latency"), the number of instructions equivalent to the

threshold value may be **determined"** . Examiner understands this to be

equivalent to the "determine the latency of a particular instruction" limitation as

recited in claim 1, and as argued by Applicant. As shown Levines is able to

monitor system for stalls and durations as well as provide a means to save

monitored information and is able to determine processor cycles per instruction

of the system.

(2) In claims 11-14,24-26,37-39, Applicant also argues for lack of

motivation to combine primary and secondary prior art.

Response (2): Examiner believes that there is a suggestion for combining

the prior art. Both references deal with profiling information dealing with object

code, so both references in are analogous art. In column 5, lines 46 – 56, of

Krishnaswamy disclose execution and profiling of object code information.

Futhermore, Krishnaswamy shows with an interpreter 27, which is combined with

Primary reference Levine to produce Applicants claim.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the

extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire

THREE MONTHS from the mailing date of this action. In the event a first

reply is filed within TWO MONTHS of the mailing date of this final action

and the advisory action is not mailed until after the end of the THREE-

MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee

pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the

advisory action. In no event, however, will the statutory period for reply

expire later than SIX MONTHS from the mailing date of this final action.

Correspondence Information

8. Any inquires concerning this communication or earlier

communications from the examiner should be directed to Chuck O.

Kendall who may be reached via telephone at (703) 308-6608.

The examiner can normally be reached Monday through Friday
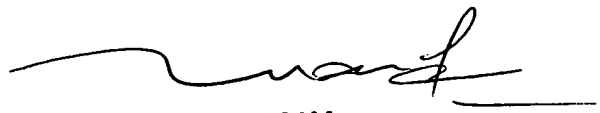
between 8:00 A.M. and 5:00 P.M. est.

If attempts to reach the examiner by telephone are

unsuccessful, the examiner's supervisor, Tuan Dam can be reached at

(703) 305-4552.

Any inquiry of a general nature or relating to the status of this

application or proceeding should be directed to the Group

receptionist whose telephone number is (703) 305-3900.

For facsimile (fax) send to central FAX number 703-872-

9306 and 703-7467240 draft.

Chuck O. Kendall

Software Engineer Patent Examiner

TUAN DAM
SUPERVISORY PATENT EXAMINER